We claim:

1. A memory cell comprising:

a semiconductor component having semiconductor material and a top side, said semiconductor component selected from the group consisting of a semiconductor body and a semiconductor layer;

a memory transistor including a source region and a drain region that are formed in said semiconductor material, said memory transistor including a gate electrode located on said top side and located between said source region and said drain region;

a dielectric material separating said gate electrode from said semiconductor material; and

a layer sequence including boundary layers and a memory layer located between said boundary layers, said layer sequence located at least between said source region and said gate electrode and at least between said drain region and said gate electrode.

2. The memory cell according to claim 1, wherein one of said boundary layers faces said semiconductor material and at least said boundary layer that faces said semiconductor material is

made of a material with a relative dielectric constant of at least 3.9.

3. The memory cell according to claim 1, wherein one of said boundary layers faces said semiconductor material and at least said boundary layer that faces said semiconductor material is made of a material with a relative dielectric constant of at least 7.8.

4. The memory cell according to claim 1, wherein one of said boundary layers faces said semiconductor material and at least said boundary layer that faces said semiconductor material is made of a material with a relative dielectric constant of at least 20.

5. The memory cell according to claim 1, wherein a barrier level of at least 2 eV is present between said semiconductor material and said memory layer.

6. The memory cell according to claim 1, wherein at least one of said boundary layers includes a material that is selected from the group consisting of an oxide and a silicate.

7. The memory cell according to claim 1, wherein at least one of said boundary layers includes a material that is selected from the group consisting of a nitride and an oxynitride.

8. The memory cell according to claim 1, wherein at least one of said boundary layers includes a material that is selected from the group consisting of Al_2O_3 and Ta_2O_5.

9. The memory cell according to claim 1, wherein said memory layer is a material that is selected from the group consisting of undoped silicon, tantalum oxide, tantalate, hafnium silicate, hafnium oxide, titanium oxide, titanate, zirconium oxide, lanthanum oxide and aluminum oxide.

10. The memory cell according to claim 1, wherein said memory layer is a material that is selected from the group consisting of tantalum oxide and tantalate.

11. The memory cell according to claim 1, wherein said memory layer is a material that is selected from the group consisting of hafnium silicate and hafnium oxide.

12. The memory cell according to claim 1, wherein said memory layer is a material that is selected from the group consisting of titanium oxide and titanate.

13. The memory cell according to claim 1, wherein said memory layer is a material that is selected from the group consisting of zirconium oxide, lanthanum oxide, and aluminum oxide.

14. The memory cell according to claim 1, wherein said semiconductor material has a trench formed therein and said gate electrode is located in said trench.

15. The memory cell according to claim 14, wherein one of said boundary layers faces said semiconductor material and at least said boundary layer that faces said semiconductor material is made of a material with a relative dielectric constant of at least 3.9.

16. The memory cell according to claim 14, wherein one of said boundary layers faces said semiconductor material and at least said boundary layer that faces said semiconductor material is made of a material with a relative dielectric constant of at least 7.8.

17. The memory cell according to claim 14, wherein one of said boundary layers faces said semiconductor material and at least said boundary layer that faces said semiconductor material is made of a material with a relative dielectric constant of at least 20.

18. The memory cell according to claim 14, wherein a barrier level of at least 2 eV is present between said semiconductor material and said memory layer.

19. The memory cell according to claim 14, wherein at least one of said boundary layers includes a material that is selected from the group consisting of an oxide and a silicate.

20. The memory cell according to claim 14, wherein at least one of said boundary layers includes a material that is selected from the group consisting of a nitride and an oxynitride.

21. The memory cell according to claim 14, wherein at least one of said boundary layers includes a material that is selected from the group consisting of Al_2O_3 and Ta_2O_5.

22. The memory cell according to claim 14, wherein said memory layer is a material that is selected from the group consisting of undoped silicon, tantalum oxide, tantalate, hafnium silicate, hafnium oxide, titanium oxide, titanate, zirconium oxide, lanthanum oxide and aluminum oxide.

23. The memory cell according to claim 14, wherein said memory layer is a material that is selected from the group consisting of tantalum oxide and tantalate.

24. The memory cell according to claim 14, wherein said memory layer is a material that is selected from the group consisting of hafnium silicate and hafnium oxide.

25. The memory cell according to claim 14, wherein said memory layer is a material that is selected from the group consisting of titanium oxide and titanate.

26. The memory cell according to claim 14, wherein said memory layer is a material that is selected from the group consisting of zirconium oxide, lanthanum oxide, and aluminum oxide.

27. A memory cell configuration, comprising:

a semiconductor component having semiconductor material and a top side, said semiconductor component selected from the group consisting of a semiconductor body and a semiconductor layer;

a plurality of memory cells that each include:

a memory transistor including a source region and a drain region that are formed in said semiconductor material, said memory transistor including a gate electrode located on said top side and located between said source region and said drain region;

a dielectric material separating said gate electrode from said semiconductor material; and

a layer sequence including boundary layers and a memory layer located between said boundary layers, said layer sequence located at least between said source region and said gate electrode and at least between said drain region and said gate electrode; and

a plurality of conductor tracks defining word lines, said gate electrode of each one of said plurality of said memory cells electrically conductively connected to one of said plurality of said conductor tracks;

said source region of one of said plurality of said memory cells defining said drain region of an adjacent one of said plurality of said memory cells and said drain region of said one of said plurality of said memory cells defining said source region of another adjacent one of said plurality of said memory cells.

28. The configuration according to claim 27, wherein:

said top side of said semiconductor material defines a top surface; and

said layer sequence is applied completely over said top surface of said semiconductor material that is between said semiconductor material and said gate electrode of each one of said plurality of said memory cells and that is between said semiconductor material and said plurality of said conductor tracks.

29. The configuration according to claim 27, wherein:

said semiconductor material has a plurality of trenches formed therein and said plurality of said trenches define walls;

said gate electrode of at least one of said plurality of said memory cells is located in one of said plurality of said trenches;

said memory layer is interrupted between a structure selected from the group consisting of said walls of one of said trenches and adjacent ones of said trenches.

30. The configuration according to claim 27, wherein:

said semiconductor material has a plurality of trenches formed therein;

said gate electrode of each one of said plurality of said memory cells is located in a respective one of said plurality of said trenches; and

each one of said plurality of said trenches is shaped in a manner selected from the group consisting of being V-shaped and shaped with obliquely oriented walls formed in said semiconductor material.

31. The configuration according to claim 27, wherein said source region and said drain region of one of said plurality of said memory cells are spaced at most 180 nm apart.

32. The configuration according to claim 27, wherein said source region and said drain region of one of said plurality of said memory cells are spaced at most 150 nm apart.

33. A method for fabricating at least one memory cell, which comprises:

etching a number of trenches in a semiconductor component that is selected from the group consisting of a semiconductor body and a semiconductor layer;

selecting the number of the trenches from the group consisting of a single trench and a plurality of trenches that run parallel to each other;

producing the number of the trenches to laterally adjoin doped regions that include a source, a drain, and at least one bit line;

fabricating a storage medium in the number of the trenches;

introducing an electrically conductive material, which is provided for a respective gate electrode, into the number of the trenches and patterning at least one conductor track on the conductive material; and

providing the at least one conductor track as a word line.

34. The method according to claim 33, which comprises, before performing the storage medium step:

filling the trenches with an oxide and implanting a dopant to form the doped regions;

providing the number of the trenches as STI trenches for electrical insulation; and

covering a section of the number of the trenches with a mask and removing the oxide at least in regions that are intended for a gate electrode.

35. The method according to claim 34, which comprises, fabricating the storage medium by applying a layer sequence including a lower boundary layer, a memory layer, and an upper boundary layer.

36. The method according to claim 33, which comprises, fabricating the storage medium by applying a layer sequence including a lower boundary layer, a memory layer, and an upper boundary layer.

37. The method according to claim 36, which comprises, between the steps of fabricating the storage medium and introducing the electrically conductive material:

removing the upper boundary layer and the memory layer, at least down to the lower boundary layer and at least between locations selected from the group consisting of walls of the number of the trenches and adjacent ones of the number of the trenches.

38. The method according to claim 33, which comprises, before fabricating the storage medium:

filling the number of the trenches with a dielectric material;

using a mask to produce openings in the dielectric material; and

performing the step of introducing the electrically conductive material such that the electrically conductive material is introduced into the openings.

39. The method according to claim 33, which comprises:

before fabricating the storage medium:

filling the number of the trenches with a dielectric material;

applying a layer of a dielectric material;

fabricating a number of openings in the layer of the dielectric material;

selecting the number of the openings from the group consisting of a single opening having a strip form and a plurality of openings that are in strip form and that are

oriented parallel to one another and transversely with respect to the number of the trenches; and

performing the step of introducing the electrically conductive material such that the electrically conductive material is introduced into the number of the openings.